ABSTRACT OF THE DISCLOSURE

STRUCTURE FOR UPDATING A BLOCK OF MEMORY ELLS IN A FLASH MEMORY DEVICE WITH ERASE AND PROGRAM OPERATION REDUCTION

An electronic circuit structure for updating a block of memory cells in a flash memory device, the memory cells storing a current value, wherein the structure includes a data latch for receiving a new value to be written on the memory cells, a controller for erasing the block of memory cells simultaneously, and programming load bank coupled to the controller and the data latch for programming the memory cells individually; the structure further includes control logic coupled to the controller for enabling the controller and for enabling the programming load bank according to a comparison between the new value and the current value.